CLAIMS:

1. Apparatus for detecting a predetermined pattern of bits in a data bitstream, the apparatus comprising:

a number of detecting elements coupled in a series configuration corresponding to a predetermined bit in the predetermined pattern of bits, each detecting element configured to present an output configured to indicate a number of mismatches between (i) the data bit received at the first input in a current detecting element and (ii) the corresponding predetermined bit in the predetermined pattern of bits received at the second input in previous detecting elements.

2. The apparatus according to claim 1, wherein each of the detecting elements comprises:

a data input configured to receive the data bitstream,

a first input configured to receive a data bit from the data bitstream,

a second input configured to receive the corresponding predetermined bit in the predetermined pattern of bits,

a third input configured to receive an error signal from a previous detecting element in the series, and

a fourth input configured to receive a clock signal; and

an output coupled to the third input of a next detecting element in the series, configured to generate said output.

3. The apparatus according to claim 1, wherein the output is further indicative of the current detecting element in the current clock cycle and the previous detecting elements in previous clock cycles.

4. The apparatus according to claim 1, further comprising:

a logic control element coupled to the output of the final detecting element of the series and configured to detect if a predetermined maximum allowed number of mismatches is detected.

5. The apparatus according to claim 4, wherein said logic control element is further configured to provide a logical output configured to indicate if the predetermined pattern of bits in the bitstream is detected when the predetermined maximum allowed number of mismatches is detected.

6. The apparatus according to claim 5, wherein the logic control element further comprises a second input configured to receive a signal indicating the predetermined maximum allowed number of mismatches.

7. The apparatus according to claim 1, wherein each detecting element comprises:

a comparator having a first input coupled to the first input of the detecting element, a second input coupled to the second input of the detecting element, and an output providing a signal indicative of whether the data bit and the corresponding predetermined bit in the predetermined pattern of bits matched or mismatched.

8. The apparatus according to claim 7, wherein each detecting element further comprises:

a combinational logic element having a first input coupled to the output of the comparator, a second input coupled to the third input of the detecting element, and an output configured to provide the output.

9. The apparatus according to claim 8, wherein each detecting element further comprises:

a register having a first input coupled to the output of the combinational logic element, a second input couple to the clock input of the detecting element, and an output configured to provide the output at the first input at the next clock cycle.

10. The apparatus according to claim 1, wherein the series of detecting elements is divided into a number of sets of detecting elements, each set having a predetermined number of detecting elements, the apparatus further comprising a serial to parallel converter coupled between the input to the apparatus and the series of detecting

elements to convert the data bitstream into sequences of bits, each sequence having the same number of bits as the number of detecting elements in each set.

11. The apparatus according to claim 1, wherein the each outputs of said detect elements comprises an error signal.

12. An apparatus configured to detect a predetermined pattern of bits in a data bitstream, comprising:

means for applying a data bit from the data bitstream to each detecting element in a series of detecting elements, each detecting element in the series corresponding to a predetermined bit in the predetermined pattern;

means for applying to each detecting element in the series of detecting elements the corresponding predetermined bit in the predetermined pattern of bits; and

means for generating, in each detecting element in the series of detecting elements an error signal indicative of the number of mismatches between the received data bit and the corresponding predetermined bit in the predetermined pattern in previous detecting elements in the series in previous clock cycles and in the current detecting element in the current clock cycle.

13. A method of detecting a predetermined pattern of bits in a data bitstream, the method comprising the steps of:

(A) applying a data bit from the data bitstream to each detecting element in a series of detecting elements, each detecting element in the series corresponding to a predetermined bit in the predetermined pattern;

(B) applying to each detecting element in the series of detecting elements the corresponding predetermined bit in the predetermined pattern of bits; and

(C) generating in each detecting element in the series of detecting elements an error signal indicative of the number of mismatches between the received data bit and the corresponding predetermined bit in the predetermined pattern in previous detecting elements in the series in previous clock cycles and in the current detecting element in the current clock cycle.

14. The method according to claim 13, further comprising the step of:

receiving the data bitstream.

15. The method according to claim 13, further comprising the step of:

applying an error signal from a previous detecting element in the series to each detecting element in the series of detecting elements.

16. The method according to claim 13, further comprising the step of:

detecting that a predetermined maximum allowed number of mismatches has been detected; and

17. The method according to claim 13, further comprising the step of:

providing an indication that the predetermined pattern of bits in the bitstream has been detected when the predetermined maximum allowed number of mismatches is detected.

18. The method according to claim 13, further comprising the step of:

receiving a signal indicating the predetermined maximum allowed number of mismatches.

19. A computer readable medium configured to store and execute the steps of claim 13.